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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/682,131	07/25/2001	Shohhei Fujio	JP920000229	2739

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EXAMINER
CHU, CHRIS C

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 01/16/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/682,131	FUJIO ET AL.	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1 - 10 is/are pending in the application.

4a) Of the above claim(s)-_____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1 - 10 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☒ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Information Disclosure Statement

1. The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A(1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 2 and 3 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 2, it cannot be determined what the applicant regards as the "wherein a first plane facing a printed circuit board for mounting electronic parts and a second plane facing opposite to said printed circuit board for mounting electronic parts in said semiconductor

integrated circuit device are defined as a bottom surface and a top surface, respectively, and said ground plane extends along said bottom surface."

In claim 3, the term "substantially" is a relative term, which renders the claim indefinite. The term "substantially" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Sasaki.

Note Fig. 1 of Sasaki, where he/she shows a semiconductor integrated circuit device comprising: a die (3) connected to a ground lead (6) and a power lead (5); a ground plane (4) connected to the ground lead; a decoupling capacitor (9) having a first end and a second end (see Fig. 1), the first end connected to the ground lead and the second end connected to the power lead (see Fig. 1); and an encapsulating material (2) for encapsulating the die, the ground plane, and the decoupling capacitor (see Fig. 1).

6. Claims 1 ~ 8 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Garbelli et al.

Note Fig. 5 of Garbelli et al., where he/she shows a semiconductor integrated circuit device comprising: a die (110 in Fig. 3) connected to a ground lead (the end of 520) and a power lead (the end of 328); a ground plane (342) connected to the ground lead (see Fig. 5); a decoupling capacitor (510) having a first end and a second end (see Fig. 5), the first end connected to the ground lead and the second end connected to the power lead (see Fig. 5); and an encapsulating material (160 in Fig. 1) for encapsulating the die, the ground plane, and the decoupling capacitor (see Fig. 5).

Regarding claim 2, note Fig. 5 of Garbelli et al., where he/she shows wherein a first plane facing a printed circuit board for mounting electronic parts (read column 4, lines 5 ~ 7) and a second plane facing opposite to said printed circuit board for mounting electronic parts in said semiconductor integrated circuit device are defined as a bottom surface and a top surface (see Fig. 5), respectively, and said ground plane (342) extends along said bottom surface (see Fig. 5).

Regarding claim 3, note Fig. 5 of Garbelli et al., where he/she shows wherein said ground plane (342) extends in two dimensions substantially throughout said bottom surface (see Fig. 5).

Regarding claim 4, note Fig. 5 of Garbelli et al., where he/she shows wherein an intra-package wiring substrate comprising wirings (520, 530, etc.) for a connecting path between the ground and power leads and bonding pads (216) of the die (110 in Fig. 3) is disposed between the die (110 in Fig. 3) and the ground plane (342), and the decoupling capacitor (510) is connected to the ground plane (342) at one end and the power line (344) of the intra-package wiring substrate at the other end (see Fig. 5).

Regarding claim 5, note Fig. 5 of Garbelli et al., where he/she shows wherein the portion of the encapsulating material (160 in Fig. 1) for inserting the power lead (under 328) is connected to a power supply bonding pad of the die (110 in Fig. 3) through a bonding wire at the die-side end (see Fig. 5), and the first end of the decoupling capacitor (510) is connected to the ground plane (342) and the second end of the decoupling capacitor (510) is connected to the specified location of said portion for inserting the power lead (see Fig. 5).

Regarding claim 6, note Fig. 5 of Garbelli et al., where he/she shows wherein the specified location of the portion for inserting the power lead to which the decoupling capacitor (510) is connected is the die-side end of the portion for inserting the power lead (see Fig. 5).

Regarding claim 7, note Fig. 5 of Garbelli et al., where he/she shows wherein the ground plane (342) is connected to the die-side end of the portion for inserting the power lead into the encapsulating material (see Fig. 5).

Regarding claim 8, since Garbelli et al. does not limit the encapsulating and the layer between the die and the ground plane (or a substrate) to any particular or specific material, his/her disclosure encompasses all well known materials for the encapsulating and the layer between the die and the ground plane (or the substrate) including the layer between the die and the ground plane (or the substrate) having a lower dielectric constant than the dielectric constant of the encapsulating material.

Regarding claim 10, Garbelli et al. discloses an electronic apparatus or control apparatus comprising a semiconductor integrated circuit device according to Claim 1 (read column 1, lines 6 ~ 28). See reject of claim 1.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Garbelli et al. in view of Hernandez et al.

Garbelli et al. discloses the claimed invention except an external decoupling capacitor provided on the printed circuit electrically connected in parallel with the decoupling capacitor of the semiconductor integrated circuit device. However, Hernandez et al. discloses an external decoupling capacitor (60) provided on the printed circuit (68 and see Fig. 10B) electrically connected in parallel with the decoupling capacitor of the semiconductor integrated circuit device. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Garbelli et al. by including an external decoupling capacitor provided on the printed circuit electrically connected in parallel with the decoupling capacitor of the semiconductor integrated circuit device as taught by Hernandez et al. The ordinary artisan would have been motivated to modify Garbelli et al. in the manner described above for at least the purpose of lower decoupling loop (read column 2, lines 68).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Bhattacharyya et al., Kabumoto et al., Hundt, Suzuki et al., Khandros et al., and Takeuchi disclose a semiconductor package.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is (703) 305-6194. The examiner can normally be reached on M-F (10:30 - 7:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7382 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Chris C. Chu
Examiner
Art Unit 2815

c.c.
January 11, 2002

EDDIE LEE
SUPERVISORY PATENT EXAMINER
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